1. Most of the existing commercial operating systems support preemptive process scheduling. Please illustrate the common practice adopted by operating systems regarding how to protect a process from never returning control to the operating system (10pts).
2. Please explain why short-job-first scheduling is not suitable to time-sharing computer systems. (5pts)
3. The wait and signal procedures of semaphores could be implemented in terms of busy waiting. Please use TestAndSet instruction to implement the wait and signal procedures for binary semaphores, where TestAndSet(X) atomically sets the value of X to true and returns the original value of X. (10pts)
4. (a) Consider a computer system that has a logical address space $2^{64}$. Suppose that the page size in such a system is 4K bytes ($2^{12}$). How many entries are required in the page table if the one-level paging scheme is adopted? (3pts)
   (b) To decrease the size of page table, and thus shorten time for memory access, the multilevel paging scheme is applied. Given a 32-bit machine with page size of 512 bytes. How many levels of a paging scheme would you recommend? (2pts) How do you divide up the bits of the address for your designed scheme? (2pts) Show the address translation for your designed paging scheme. (3pts)
5. (a) Draw figures to explain the following two allocation methods of disk space: (I) (3pts) the use of file allocation table; (II) (3pts) indexed allocation.
   (b) Consider the following page reference string: 7, 0, 1, 2, 0, 3, 0, 4, 2, 3, 0, 3, 2, 1. How many page faults would occur on the following page replacement algorithms? Assume that there are three frames in the memory. (I) The LRU algorithm (3pts); (II) The FIFO algorithm (3pts); (III) The Optimal Replacement algorithm (3pts)
6. (25 pts) A pipelined processor architecture consists of 5 pipeline stages: Instruction Fetch (IF), Instruction Decode and Register Read (ID), Execution or Address calculation (EX), Data Memory Access (MEM), and Register Write Back (WB). The delay of each stage is summarized below: IF = 2 ns, ID = 1.5 ns, EX = 4ns, MEM = 2.5 ns, WB = 2 ns.
   (a)What's the maximum attainable clock rate of this processor?
   (b)What kind of instruction sequence will cause data hazard that cannot be resolved by forwarding? What's the performance penalty?
   (c) To improve on the clock rate of this processor, the architect decided to add one pipeline stage. The location of the existing pipeline registers cannot be changed. Where should this pipeline stage be placed? What's the maximum clock rate of the 6-stage processor? (Assuming there is no delay penalty when adding pipeline stages)
   (d) Repeat the analysis in (b) for the new 6-stage processor. Is there other type(s) of instruction sequence that will cause a data hazard, and cannot be resolved by forwarding? Compare the design of 5-stage and 6-stage processor, what effect does adding one pipeline stage has on data hazard resolution?
7. (10 pts) (a) What type of cache misses (compulsory, conflict and capacity) can be reduced by increasing the cache block size? (b) Can increasing the degree of the cache associativity always reduce the average memory access time? Explain your answer.
8. (10 pts) List two types of cache write policies. Compare the pros and cons of these two polices.
9. (5 pts) Briefly describe the difference between synchronous and asynchronous bus transaction.