※注意：作答時，請於答案卷上標明作答之大題及其題號，並依序作答。

一、單選選擇題(20%，每題 2%，不倒扣，答案卷上需按題序答題，否則不予計分)

1. Which one of the following is true for an ideal op amp? (a) $R_{in} = 0$ and $R_{out} = 0$ (b) $R_{in} = \infty$ and $R_{out} = \infty$ (c) $R_{in} = \infty$ and $R_{out} = 0$ (d) $R_{in} = 0$ and $R_{out} = \infty$.

2. For the amplifier shown in Fig. 1, which one of the following is a correct approach to increase the small-signal voltage gain? (a) decrease W/L of M_1 (b) increase W/L of M_2 (c) decrease I_{BIAS} (d) decrease channel lengths M_1 and M_2.
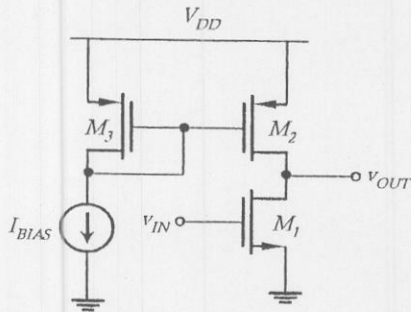

Fig. 1

3. For the amplifier shown in Fig. 2, which one of the following is NOT true if the value of R_E increases: (a) input resistance increases (b) output resistance increases (c) transconductance increases (d) the negative feedback is enhanced.
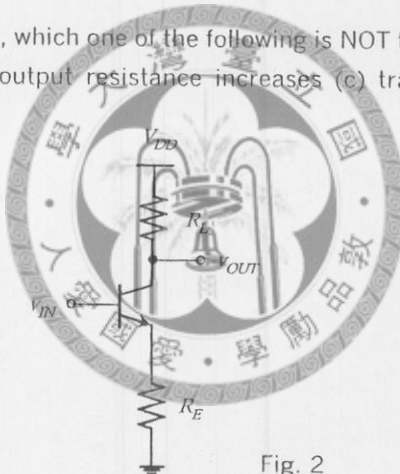

Fig. 2

4. Which of the following is NOT an advantage of negative feedback? (a) Desensitize the gain, (b) Extend the bandwidth, (c) Increase the gain, (d) Reduce nonlinear distortion.

5. If a Class B power amplifier is at the point of maximum power dissipation, its power conversion efficiency will be (a) 0 % (b) 25 % (c) 50 % (d) 78.5 %.

6. If a BJT has $I_C = 1$ mA, $f_T = 400$ MHz, and $C_\pi = 10.9$ pF (EB junction capacitance), its C_μ (CB junction capacitance) = (a) 2 pF, (b) 3 pF, (c) 4 pF, (d) 5 pF.

7. The second-order filter using the op-amp-RC resonator, as shown in Fig. 3, has a function of (a) high-pass, (b) notch at ω_0, (c) band-pass, (d) all-pass.
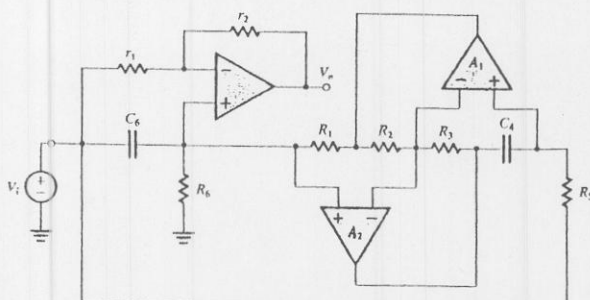

Fig. 3

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8. The equivalent input resistance at point ν of Fig. 4 is (a) R_f, (b) $-R_f$, (c) $2R_f$, (d) $-2R_f$.
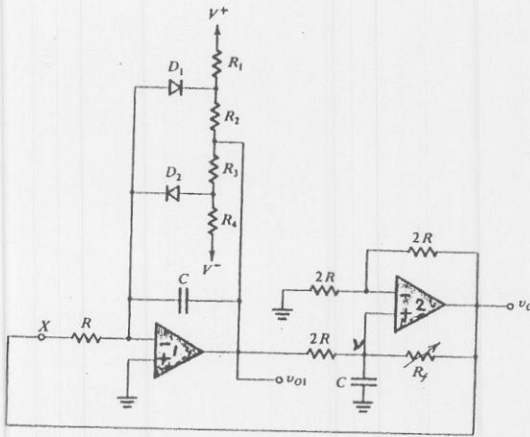

Fig. 4

9. The minimum number of transistors to realize the Boolean function of AB+BC+CA in full CMOS logic gate circuits is (a) 6, (b) 10, (c) 18, (d) none of the above.

10. Which of the following logic circuit cannot pull the output high level to V_{dd} (the highest voltage supply)?
    (a) TTL, (b) CMOS, (c) NMOS (depletion load), (d) none of the above.

二、計算、問答題

1. (12%) Consider the circuit in Fig. 5, in which $R_1 = R_2 = R_3 = R_4 = R_5 = R_6 = 10K\Omega$, $V_{DD} = 5V$ and $V_i = 3V$.
   (a) (4%) Assume the Op Amps have infinite gain. What are the values of current I_1 and I_2?
   (b) (8%) Find the current I_1 and I_2 again using Op Amps with a finite gain (A = 10) for the same circuit.

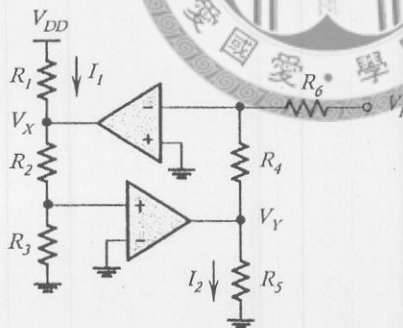

Fig. 5

2. (8%) Consider the circuit in Fig. 6. Use the following parameters for calculation: $V_{DD} = 5V$, Input DC bias = 3V, $I_{BIAS} = 300\mu A$, $\mu_n C_{ox} W_1/L_1 = \mu_p C_{ox} W_2/L_2 = \mu_p C_{ox} W_3/L_3 = \mu_p C_{ox} W_4/L_4 = 200 \ \mu A/V^2$, $V_{TN} = 1V$ and $V_{TP} = -1V$.
   (a) (4%) What is the output DC voltage of the circuit?
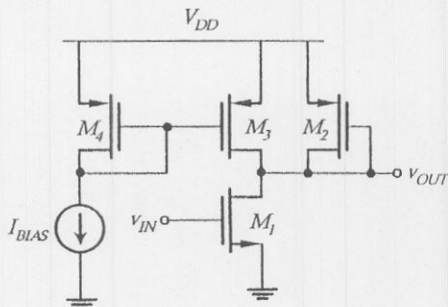   (b) (4%) Find the small-signal voltage gain of the amplifier.

Fig. 6

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3. (20%) Fig. 7 shows a folded cascode amplifier. The base of Q_2 is fixed at V_{BIAS}. V_A (Early voltage), β, C_π, and C_μ of all transistors are identical. In the circuit, $R_s = 2.5$ kΩ, $I = 1$ mA, $V_T = 25$ mV (thermal voltage), $V_A = 50$ V, $\beta = 50$, $C_\pi = 12$ pF, and $C_\mu = 2$ pF.

   (a) (10%) Assume the output resistances of the two current sources are infinity. Find the output resistance R_o and the mid-band voltage gain v_o/v_i of this amplifier.

   (b) (5%) The common emitter stage of the amplifier uses a PNP BJT, i.e., Q_1. Calculate the pole frequency (in Hz) at the input side of Q_1.

   (c) (5%) The total capacitance at the output node is $C_L = 20$ pF. Find the pole frequency (in Hz) at the output node.

Fig. 7
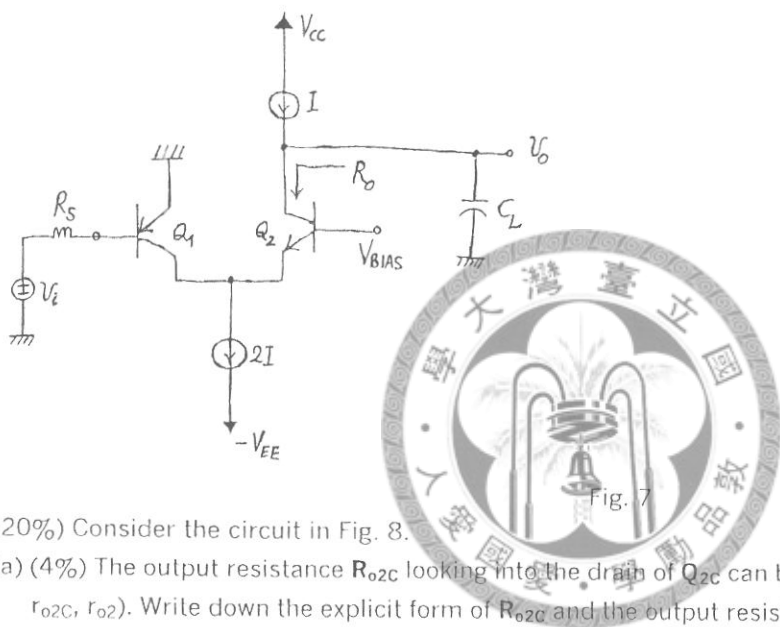
4. (20%) Consider the circuit in Fig. 8.

   (a) (4%) The output resistance R_{o2c} looking into the drain of Q_{2c} can be expressed as a function of $f(g_{m2}, r_{o2c}, r_{o2})$. Write down the explicit form of R_{o2c} and the output resistance R_o of the first stage of CMOS Op Amp.

   (b) (16%) Let $2I = 25\,\mu$A; $\mu_n C_{ox} = 20\,\mu$A/V^2; $\mu_p C_{ox} = 10\,\mu$A/V^2; $|V_t| = 1$V; $|V_A| = 25$V; W/L for Q_1, Q_{1C}, Q_2, and $Q_{2C} = 120/8$; W/L for Q_{3C} and $Q_{4C} = 60/8$; W/L for Q_3 and $Q_4 = 8/8$. Calculate numerical values of the output resistance and voltage gain of the first stage.
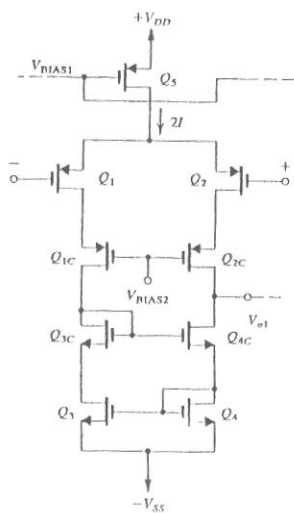

Fig. 8

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5. (20%) In the standard TTL inverter shown in Fig. 9(a), the voltage transfer characteristic curve looks like the one shown in Fig. 9(b).

(a) (8%) analyze the operation modes of transistors Q1, Q2, Q3, Q4 and voltages at their collectors when input voltage $V_I = 5V$.

(b) (3%) explain the function of the diode D at the output stage.

(c) (6%) estimate the coordinates (V_I, V_O) of points B and C and the slope of the BC segment in Fig. 9(b).

(d) (3%) explain how the BC transition region in Fig. 9(b) can be removed by replacing the 1 kΩ resistor with an "active pull-down" circuit.
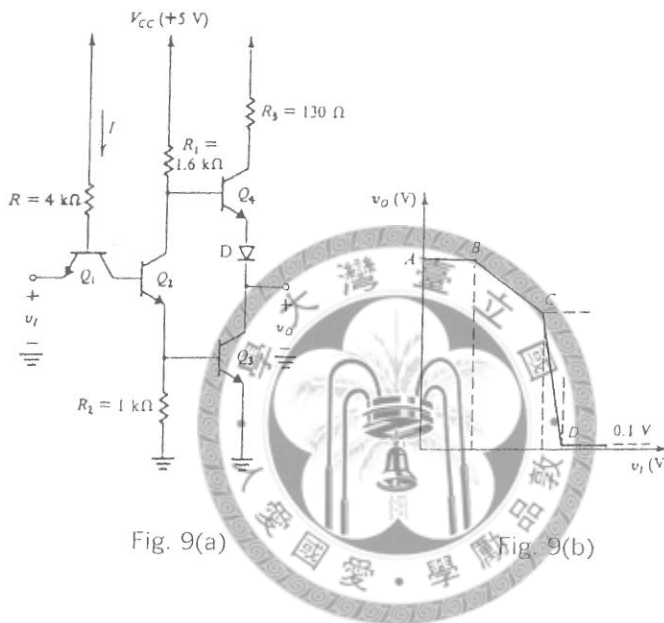
Fig. 9(a)   Fig. 9(b)

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