國立台灣大學九十三學年度碩士班招生考試試題

科目：電子學(甲)　　題號：460

一、單選選擇題(20%, 每題 2%, 不倒扣, 答案卷上需按題序答題, 否則不予計分)

1. For an amplifier, the input resistance is 100 ohm, the output resistance is 2 ohm, and the load resistance is 5 ohm. If the input voltage of the amplifier is 0.1V, the output voltage of the amplifier is 1V. What is the transconductance gain of the amplifier? (a) 30 dB (b) 6 dB (c) 20 dB (d) 23 dB (e) none of the above.
2. By increasing the reverse bias voltage of a pn junction diode (before breakdown), the junction capacitance will (a) increase (b) decrease (c) not change (d) increase first, then decrease (e) decrease first, then increase.
3. Which device in the following is most suitable to make a simple and stable voltage reference circuitry? (a) BJT (b) NMOSFET (c) PMOSFET (d) JFET (e) GaAs MESFET.
4. Which of the following statements is NOT true? (a) For a stable circuit, poles must locate in the left-hand side of s-plane; (b) if the Nyquist Plot encircles the point (-1, 0), the system is stable; (c) a negative feedback system reduces the nonlinearity; (d) a class B output stage provides a maximum power efficiency of $\pi/4$.
5. Which of the following statements is NOT true? (a) The offset voltage of a bipolar differential pair is typically smaller than that of a CMOS differential pair; (b) a class AB stage eliminates the dead zone by establishing turn-on voltages with small quiescent current; (c) a system oscillates if the poles are on the $j\omega$ axis or in the right-hand side of s-plane; (d) in a Bode Plot, a zero located in the right-hand side of s-plane increases the magnitude slope by 20 dB/dec and raises the phase by 90°.
6. Which of the following statements is NOT true? (a) Cascode configuration achieves a high gain by increasing the output resistance; (b) BiCMOS technology combines bipolar and CMOS devices, providing the advantages of these two technologies; (c) Conventional Op-amp circuits (e.g., the 741 Op-amp) consist of short-circuit protection in the output stage; (d) For a system with real coefficients, its poles and zeros must be real.
7. Which one of the following is NOT true for TTL logic? (a) output stage provides active pull-up (b) output stage provides active pull-down (c) input diodes are replaced by BJT (d) all transistors are non-saturated during the operation.
8. Compared with simple current mirror, which one of the following is the advantage of using cascode current mirrors? (a) power dissipation (b) output resistance (c) output swing (d) circuit complexity.
9. Which one of the following is NOT true for a BJT differential amplifier? (a) the input resistance is infinite (b) the differential transconductance (g_m) increases with the bias current (c) the gain decreases if emitter resistors R_E are added (d) CMRR can be increases by minimize the common-mode gain.
10. Which of the following is the condition for a feedback amplifier to be stable: (a) when the phase of the open-loop gain is 180°, its magnitude is <1; (b) when the phase of the closed-loop gain is 180°, its magnitude is <1; (c) when the phase of the loop gain is 180°, its magnitude is <1; (d) when the phase of the closed-loop gain is 180°, its magnitude is >1; (e) none of the above.

二、計算、問答題

1. (20%) For a doped Si bar with a pn junction at the center as shown in Fig.1, the dopant concentration is $10^{17}/cm^3$ at p-type side and $10^{20}/cm^3$ at n-type side. Please calculate
   (a) (5%) the built-in voltage of the pn junction.
   (b) (5%) the ratio of the width of depletion region at the p-side to that at the n-side ($x_p : x_n$).
   (c) (4%) the hole and electron concentration at the p-side far from the pn junction.
   (d) (6%) the resistivity at the n-side far from the pn junction assuming the diffusion constants are D_p = 12 cm^2/sec and D_n = 36 cm^2/sec, respectively.

   Use the following parameters if necessary for calculation: T = 300K , $n_i = 10^{10}/cm^3$, k = 8.617×10^{-5} eV/K, Ks (Si dielectric constant) = 11.8, $\varepsilon_o = 8.85 \times 10^{-14}$ F/cm, q = 1.6×10^{-19} coul.

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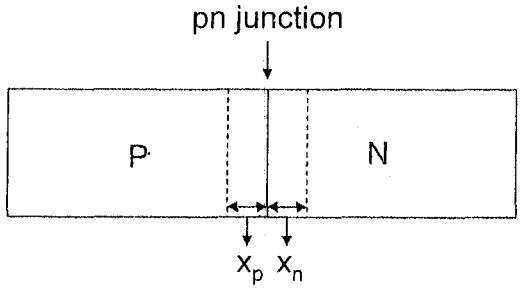

Fig. 1

2. (12%) Consider the circuit shown in Fig. 2(a). The circuit is perfectly symmetric and properly biased with common-mode feedback so that all transistors operate at saturation region. The dimensions of NMOS and PMOS transistors are chosen such that $\mu_n C_{ox}(W/L)_n = \mu_p C_{ox}(W/L)_p = 0.1$ A/V^2, and the capacitance at nodes P and Q and outputs are lumped as C_E = 0.1 pF and C_L = 0.5 pF. The tail current source I_{SS1} and I_{SS2} are equal to 1 mA and 4 mA, respectively. The output resistance for $M_{1\text{-}8}$ is 1 kΩ whereas that of $M_{9\text{-}12}$ is 2 kΩ. Neglect other capacitance and body effect.

(a) (8%) Calculate the input and output resistance, voltage gain at low frequencies, poles at nodes P (or Q) and output nodes. Depict the frequency response (Bode Plot) and find the phase margin

(b) (4%) Now a capacitor C_C is introduced between the output nodes and all the other conditions remain unchanged, as shown in Fig. 2(b). Find the value of C_C that makes the phase margin equal to 45°.

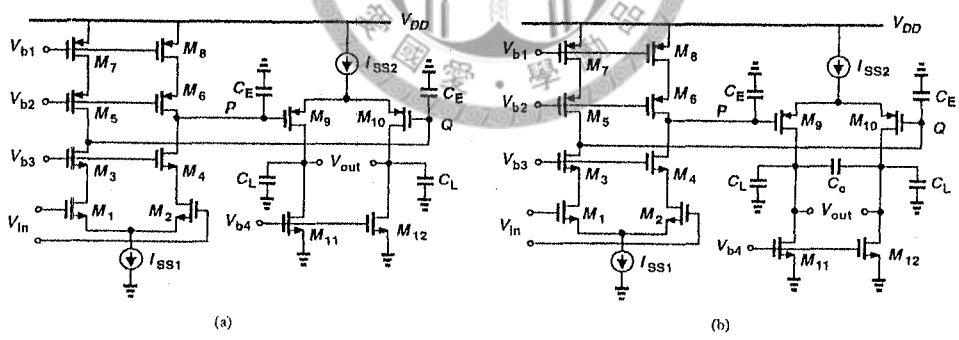

Fig. 2

3. (8%) A transimpedance amplifier is shown in Fig. 3. Assume current sources I_1, I_2, and I_3 are ideal, and the transconductance and output resistance of transistor M_1, M_2, and M_3 are g_{m1}, g_{m2}, g_{m3} and r_{O1}, r_{O2}, r_{O3}, respectively. Determine the closed-loop transimpedance gain (V_{out}/I_{in}) and the input and output impedances. Simplify the expressions for channel-length modulation coefficient $\lambda \to 0$.

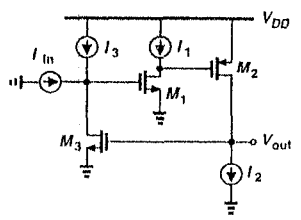

Fig. 3

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4. (20%) Fig. 4(a) shows the circuit of an astable multivibrator using CMOS inverters. The voltage transfer characteristics of the inverter is also shown in Fig. 4(b). You are given the ideal approximations that: (i) the clamping diodes at the logic gate inputs are ideal and have a turn-on voltage of V_D. (ii) the output resistances of the CMOS inverters are nearly zero

   (a) (8%) Give the waveform of V_{I1}

   (b) (12%) and show that the period (T) of the output square waves at V_{O1} and V_{O2} is

$$T = CR \times \ln\left(\frac{V_{DD}+V_D}{V_{DD}-V_{th}} \times \frac{V_{DD}+V_D}{V_{th}}\right)$$

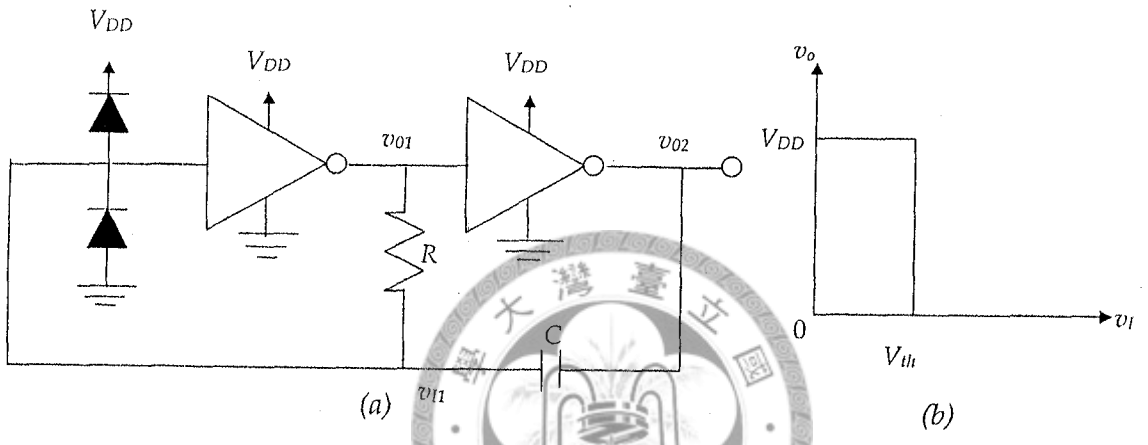

Fig. 4

5. (20%) Fig. 5 shows a differential amplifier circuit with all the transistor W/L values. The device parameters are given as $\mu_n C_{ox}$ = 20 μA/V², $\mu_p C_{ox}$ = 10 μA/V², V_{tn} = 1V, V_{tp} = -1V, and the channel length modulation effect can be neglected.

   (a) (8%) Find I_{D1}, I_{D3}, V_{D1}, and V_{D5} when the input is biased at 5V.

   (b) (4%) What is the maximum and minimum input common-mode voltage allowed for this differential amplifier?

   (c) (8%) What is the small-signal voltage gain A_{vd} (= $\frac{v_{out}}{v_{in}}$)?.

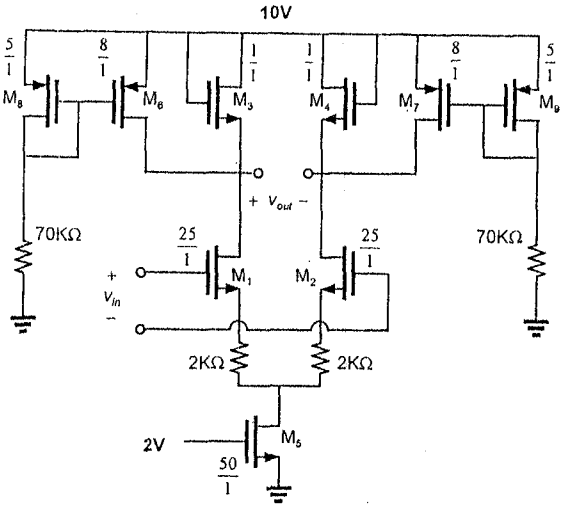

Fig. 5

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