＊ 下列題目請在試卷內的「選擇題作答區」作答。

一、單選選擇題(20%, 每題 2%, 不倒扣, 答案卷上需按題號答題, 否則不予計分)

1. Which one of the followings is NOT true for an ideal transconductance amplifier? (a) the input signal is voltage (b) the output signal is current (c) $R_i=\infty$ (d) $R_o=0$.
2. Which one of the followings is NOT true for a CMOS inverter? (a) ratioless logic (b) no static power dissipation (c) dynamic power dissipation inversely proportional to the switching frequency (d) current flows only at transition.
3. Which one is NOT true when a reverse bias is applied to a p-n junction? (a) current flows from n-type to p-type region (b) depletion-layer width increases (c) diffusion capacitance dominates (d) breakdown may take place if the reverse voltage is too high.
4. For an NMOS transistor, which of the following is NOT correct? (a) transconductance g_m is inversely proportional to drain current I_D for a given overdrive ($V_{GS}-V_t$), (b) output resistance is proportional drain current I_D, (c) output resistance is proportional to channel length, (d) current of deep-submicron devices would be restricted by carrier's velocity saturation.
5. Which of the following is NOT correct? (a) feedback can enlarge the bandwidth, (b) feedback can lower the gain sensitization, (c) feedback can increase linearity, (d) feedback can improve the noise performance.
6. Which of the following is NOT correct? (a) For a feedback system, its poles must locate at the left-hand side of the s plane, (b) a system is unstable if its Nyquist plot encircles (-1, 0), (c) in a shunt-shunt feedback, the closed-loop input and output resistance decreases by a factor of $(1+A\beta)$, (d) pole-splitting technique degrades the phase margin.
7. Which type of filter provides the most precise cut-off frequency and Q? (a) passive RLC filter (b) Antoniou Inductance-simulation circuit filter (c) Integrator-based biquad with opamp –RC (d) Single-amplifier biquad (SAB) (e) Switched-capacitor filter.
8. What is the main advantage of ECL as a logic gate? (a) Power (b) Area (c) Speed (d) Noise (e) Cost.
9. Which feature can be applied to Domino CMOS Logic? (a) Non-inverting output (b) Static logic (c) Small swing (d) Ratio logic (e) Non-zero static power.
10. A 3-input CMOS NAND gate can perform as a CMOS inverter if we connect all inputs of the NAND3 together (called i-NAND3 here). Similarly, we can form another CMOS inverter by connecting all inputs of a 3-input CMOS NOR gate together (called i-NOR3). Suppose that all NMOS and PMOS are of the same size ($W/L=2\mu m/1\mu m$, it is called *Unit-sized MOS* in this question). The delay response for an inverter pair ($t_{inv\text{-}pair}$) can be computed by the fall time of the 1st inverter (t_{fall}) and the rise time of the 2nd inverter (t_{rise}). Suppose that we have
    (i) Inverter pair formed by two inviters of unit-sized NMOS and PMOS
    (ii) Inverter pair formed by two i-NAND3 of unit-sized NMOS and PMOS
    (iii) Inverter pair formed by two i-NOR3 of unit-sized NMOS and PMOS
    Compare the delay time, $t_{inv\text{-}pair}$, of these three inverter pairs and choose your answer below: (a) (ii) > (i) > (iii). (b) (iii) > (i) > (ii). (c) (i) = (ii) = (iii). (d) None of above.

接背面

＊ 下列題目請在試卷內的「非選擇題作答區」作答。

二、計算、問答題

1. (20%) For the amplifier in Fig. 1, let $\mu_n C_{ox}=200\mu A/V^2$, $V_t=1V$, $(W/L)_1=10$, $(W/L)_2=20$, and β(for BJT)=500.

   (a) (10%) Find the DC voltage at the output.

   (b) (10%) Find the small-signal voltage gain v_o/v_i.

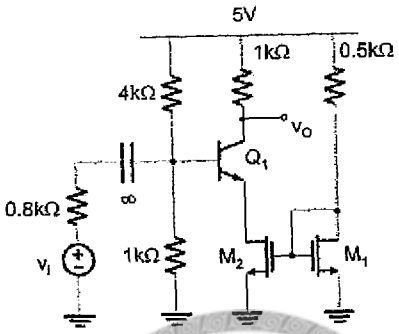
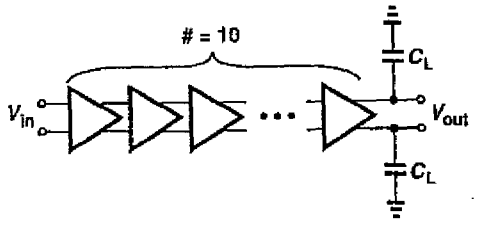


Fig. 1

2. (20%) Consider an amplifier chain of 10 identical stages as shown in Fig. 2. Each stage is realized as a differential structure, where the PMOS devices (M_3 and M_4) and tail current are properly biased (through common-mode feedback) so that all transistors are in saturation. Transistor M_1 and M_2 have $\mu nC_{ox}(W/L)=0.1$ (A/V^2), and the tail current I_{SS}=1mA. The output resistances of NMOS and PMOS devices are both equal to 2 kΩ. Also, the input $v_{in}(t)=0.1\times\cos(2\pi f_{in}t)$ (V). The load capacitance C_L is 1 pF, and other parasitics are neglected.

   (a) (10%) Determine the transfer function of the amplifier chain.

   (b) (10%) If f_{in}=10 GHz, plot the differential output waveform $V_{out}(t)$.



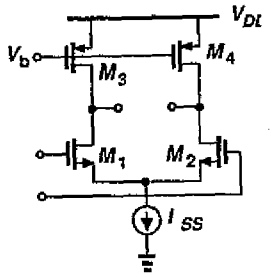


Fig. 2

3. (20%) For the following circuits in gate level (Fig. 3),

   (a) (4%) Draw a CMOS NOR gate in transistor level. Write the (W/L) ratio of PMOS and NMOS to balance the T_{PLH} and T_{PHL}.

   (b) (5%) Describe V_{OUT1} and V_{OUT2} as a function of V_{IN1} and V_{IN2} in Fig. 3-(a). You can

接次頁

use truth table to express your answer.

(c) (11%) Now, the circuit is modified as in Fig. 3-(b) and apply a periodic square clock signal at input, what do V_{OUT1} and V_{OUT2} look like? Note that T_{nr} and T_{pd0-4} are the delay for NOR gates and inverters. Additionally, Ts is much larger (at least 10 times) than T_{nr} and T_{pd0-4}.

In this problem, you must show (i) the HIGH and LOW pulse width for both outputs (ii) the "relative" relation between input and both outputs.

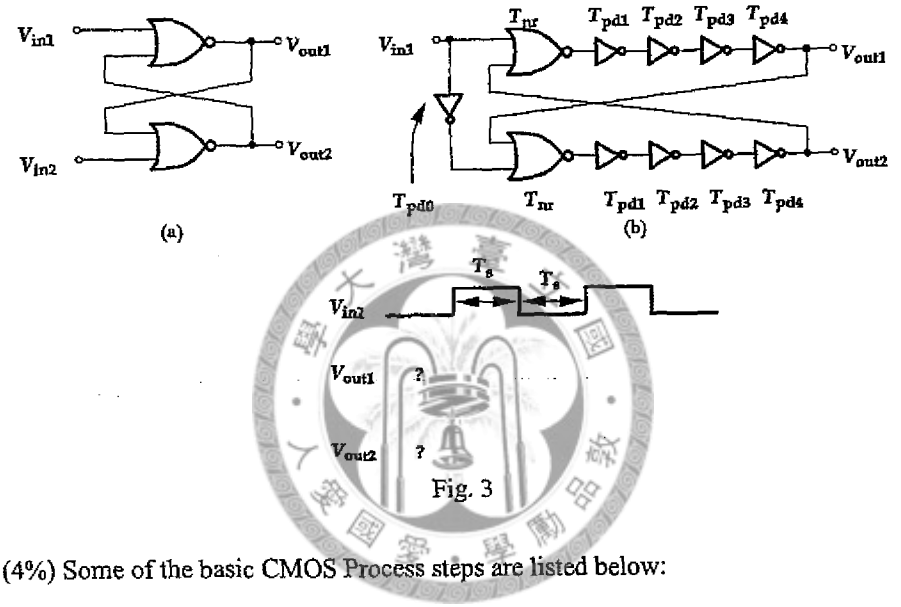


Fig. 3

4. (4%) Some of the basic CMOS Process steps are listed below:

   (a) Grow thick *Field oxide*
   (b) Polysilicon gate definition using *polysilicon mask*
   (c) Define n-well (or so-called n-tub) using *n-well mask*
   (d) Metallization using *metal mask*
   (e) Define n+ diffusion area using *n+ mask*
   (f) Define p+ diffusion area using *p+ mask*
   (g) Contact cuts definition using *contact mask*

   Write down the proper sequence of these CMOS process steps that are used to form a CMOS Inverter in a basic n-well CMOS process. That is, sort and list all 7 steps by the order that they are executed during the CMOS process (just write down the 7 process step numbers in your answer sheet).

5. (8%) The top view of a CMOS inverter layout in a basic n-well process is shown in Fig. 4(b). Now you are asked to draw the cross section of this CMOS inverter (*i.e.*, CMOS 反向器在 substrate 中的橫切面 in Fig. 4(c)). Indicate the *p-substrate, n-well, p+, n+, Vdd (supply voltage), Vss (ground), contact cut, polysilicon, metal, gate oxide,* and *field*

oxide in your plot.

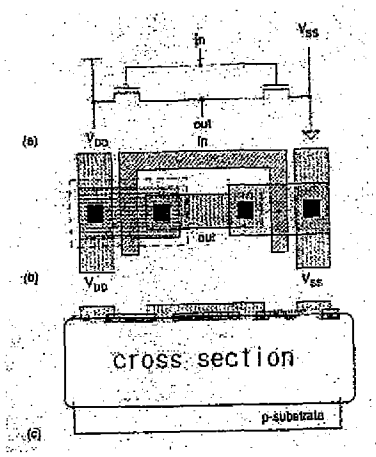


Fig. 4

6. (8%) The layout of a CMOS complex gate is shown in Fig. 5. Write down

   (a) (4%) The schematic view of this layout.

   (b) (4%) The *Truth table* and the *simplified logic function* and of ***Z=f(A,B)***.

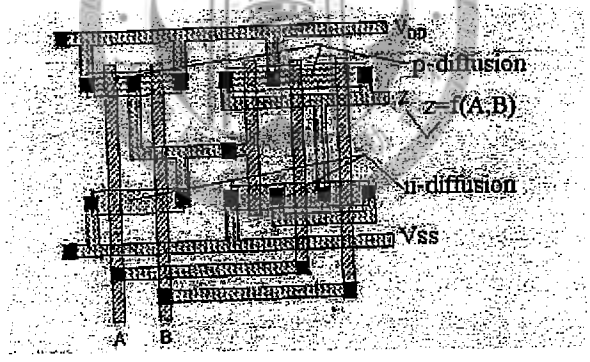


Fig. 5