1. The following calculation was performed by a particular breed of unusually intelligent chicken. If the radix r used by the chicken corresponds to its total number of toes, how many toes does the chicken have on each foot? Verify your answer. (6%)

$$(15)_r \times (24)_r - (17)_r = (365)_r$$

2. Prove the identity of each of the following Boolean equations, using algebraic manipulations. State *clearly* the theorem you use in each step. (10%)

   - $AB + BC'D' + A'BC + C'D = B + C'D$
   - $AC' + A'B + B'C + D' = (A' + B' + C' + D')(A + B + C + D')$

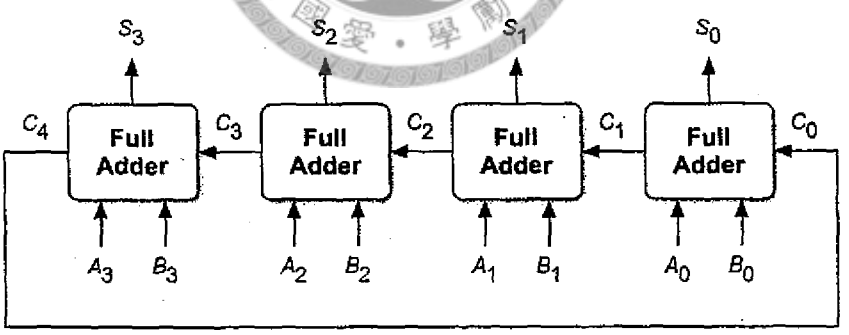
3. Find the minimum sum-of-products and the minimum product-of-sums expressions for the following function. (10%)

$$F(A, B, C, D) = \Sigma m(1, 5, 7, 10, 12, 14) + \Sigma d(0, 3, 6, 8, 9, 13)$$

4. A full adder (FA) is a combinational logic module that adds two bits (a and b) and a carry (c_{in}). Its outputs consist of a sum bit (s) and a carry (c_{out}).

   - Draw the truth table of a full adder (s and c_{out}). (4%)
   - Find an OR-AND circuit for the adder which has no hazards. (Assume that the inputs are available in both the complemented and uncomplemented forms.) (6%)

5. The following circuit is an arithmetic module.



   - What arithmetic operation does it perform? Explain why. (10%)
   - Under what circumstances does overflow occur? (8%)
   - Design a logic circuit to detect overflow. Its output V equals 1 if an overflow occurs; otherwise, V equals 0. (6%)

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6. A sequential circuit with one input and one output is used to stretch the first bit and delay the third bit of a 4-bit sequence as follows:

input (x)	output (y)
0x0x	0000
0x1x	0001
1x0x	1110
1x1x	1111

Given the input sequence $x_0x_1x_2x_3$, the output sequence is $x_0x_0x_0x_2$. After every four bits, the circuit resets. Note that the second and fourth bits of the input sequence can be either 1 or 0.

- Find a Mealy state graph and table for the circuit. Minimize the number of states. (10%)
- Draw the timing diagram of your answer using the following input sequence: (8%)

  01101101

  Assume that the circuit is positive edge triggered.
- If the input changes occur slightly after the active clock edge, indicate places in the output waveform where false outputs can occur. (6%)

7. Using edge-triggered D flip-flops, design a one-input (x) one-output (z) sequential circuit N whose state diagram is shown below. (16%)