單選題 (10 pts, 2 pts each)　　※ 注意：請於試卷上「選擇題作答區」依序作答。

1. Choose the power amplifier configuration that has the lowest power dissipation during quiescent situation (i.e., no signal input), and the highest power conversion efficiency at maximum output amplitude: (A) Class A; (B) Class B; (C) Class AB; (D) They cannot achieve both advantages.

2. Which of the following is not a function of Miller frequency compensation? (A) Bandwidth extension of the forward amplifier; (B) Feedback stability when used with external resistive feedback; (C) Efficient compensation without using large capacitor values; (D) To move the frequency location of the original dominant pole.

3. Choose the single configuration that is best suitable for implementation of CMOS static memory address decoder: (A) Pseudo NMOS NOR logic; (B) Pseudo-NMOS NAND logic; (C) CMOS NOR logic; (D) CMOS NAND logic.

4. Choose the single correct statement about common-drain-common-source cascade amplifier: (A) The common-drain stage increases the input impedance; (B) The common-source stage provides low output impedance; (C) The use of the common-drain stage provides a low-impedance node to widen the frequency bandwidth; (D) The use of common-source stage provides a current buffer to increase the open-circuit output voltage gain.

5. Choose the single incorrect statement about folded-cascode differential amplifier, as compared with cascode differential amplifier: (A) It achieves the purpose of level shifting; (B) It achieves the purpose of increased input common-mode range; (C) It is often better suited for low-voltage applications; (D) It is often much better in terms of frequency response.

接背面

※ 注意：請於試卷上「非選擇題作答區」依序作答，並應註明作答之大題及小題題號。

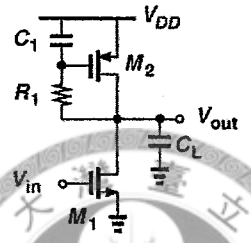
計算與問答題 (90 pts)

1. (30 pts) See figure on next page. Neglect all other capacitance and assume $\lambda = 0$.

(a) (10pts) Determine the zero of the transfer function without calculating the transfer function.

(b) (10 pts) Determine the impedance of the load consisting C_1, R_1, and M_2. (7 pts) Under what condition does the impedance become inductive? (3 pts)

(c) (10 pts) Determine the overall transfer function of the amplifier.



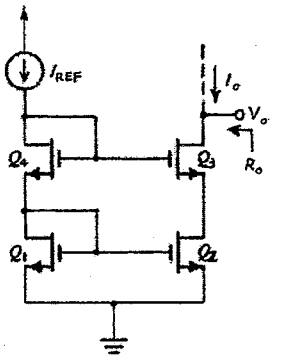
2. (30 pts) Given below is a cascode MOS current mirror circuit.

(a) (5 pts) Symbolically derive the resistance as seen from the output node. Neglect body effect for simplicity.

(b) (10 pts) With $V_{SS} = -5$ V, $I_{REF} = 10$ uA, $V_t = 1$ V, $u_nC_{ox} = 20$ uA/V^2, $L = 10$ um, $W = 40$ um, and $V_A = 20$ V. Find the output resistance and the lowest allowable output voltage. Assume all devices are equal.

(c) (10 pts) Repeat the above for an NMOS current mirror without using cascode.

(d) (5 pts) Explain the benefit of cascode current mirror and its trade-off.



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3. (21 pts) Consider the following pass-transistor logic circuit. The body effect and subthreshold current are neglected in this problem. Note that V_{tn} =0.7 V and $|V_{tp}|$ =0.6 V.

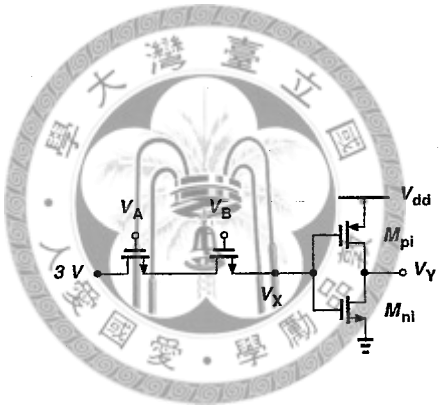
(a) (2 pts) V_A =3 V, V_B =3 V, what is the steady-state voltage for V_X?

(b) (5 pts) Repeat part (a) for (V_A =3.5 V, V_B =3 V) and (V_A =4 V, V_B =4 V)?

(c) (3 pts) A CMOS inverter (M_{ni} and M_{pi}) is added to obtain full swing at the output of V_Y. What's the maximum V_{dd} to avoid the DC leakage for the input in (a)?

(d) (5 pts) Use V_{dd} in (c) to 'design PMOS and NMOS ratio for the CMOS inverter to obtain $V_M = \frac{V_{dd}}{4}$, where V_M is defined as $V_{in} = V_{out} = V_M$.

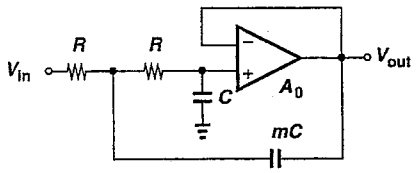
(e) (6 pts) Can we express V_Y by $Y = \overline{AB}$? If not, please add NMOS-only transistors to generate NAND function?



4. (9 pts) A single amplifier biquad filter can be implemented as the following circuit. The open-loop gain of the amplifier is A_0 but not infinite.

(a) (2 pts) What type of filter is it? low pass or ?

(b) (7 pts) Derive the transfer function and obtain Q and ω_0.



試題隨卷繳回