1. Fig.1 shows the schematic of an instrumentation amplifier with $R_2 = R_3 = R_4 = 100$ kΩ, and $2R_1 = 10$ kΩ. All Ops are ideal. Please answer the following questions.
   (a) difference-mode gan; (12 pts)
   (b) common-mode gain; (12 pts)
   (c) CMRR. (10 pts)

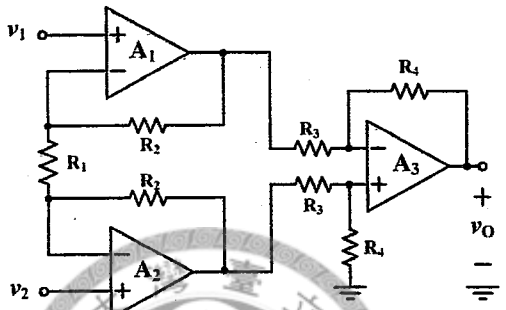

Fig.1

2. Assume all the transistors in Fig.2 have the same characteristics. If $\beta = 200$, $V_A = 100$V, T = 290K, $V_{cc} = 5$V, $R_1 = 10$ kΩ and $R_2 = 11$ kΩ, please solve the following questions. (Note: no points will be given if the problem-solving procedures are not shown)
   (a) common-mode voltage gain (A_{cm}); (5 pts)
   (b) differential voltage gain (A_d); (5 pts)
   (c) CMRR; (3 pts)
   (d) Differential input resistance (R_{id}). (5 pts)

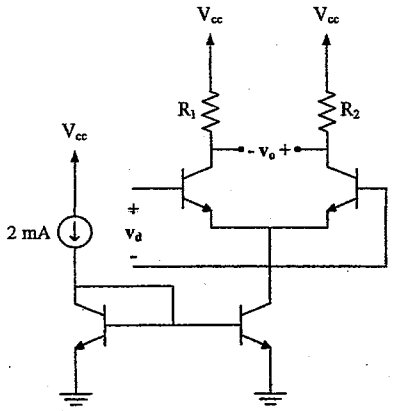

Fig.2

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3. Assume that the two transistors (Q_1 and Q_2) in Fig.3 are operating in the saturation region with different g_m (g_{m1}, g_{m2}) and r_o (r_{o1}, r_{o2}). Please find the following circuit characteristics. The body effect can be neglected for simplicity but the transistor output resistance (r_o) needs to be included in the analysis.
   (a) Input resistance (R_{in}); (5 pts)
   (b) Output resistance (R_{out}); (5 pts)
   (c) Small-signal open-circuit voltage gain (v_o/v_{in}). (5pts)

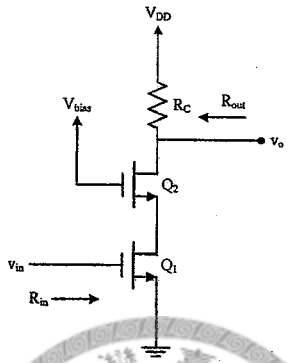

Fig.3

4. For the circuit below (see Fig.4), OP_1 is an ideal opamp, V_1 and V_2 are ideal DC voltage sources, all PMOS transistors have the same size of $(W/L)_P$, and all NMOS transistors are the same with size of $(W/L)_N$. Assume the drain voltages of transistors P_5 and N_3 are biased properly. The threshold voltages of PMOS and NMOS are V_{tp} and V_{tn}, respectively. Assume $(W/L)_P=2(W/L)_N=(W/L)$, $|V_{tp}|=V_{tn}=V_t$, and $k_n'=2k_p'=k$ ($k_n'=\mu_n C_{ox}$ and $k_p'=\mu_p C_{ox}$). Ignore the channel-length modulation and body effect.

(a) If $R_a=R_b=0$, derive an equation for the drain current (I_1) of transistor N_1 in terms of the circuit and device parameters. (4 pts)

(b) Continue from (1), if V_1=4V, V_2=1V, R_1=3kΩ, (W/L)=200, V_t=0.5V, k=100μA/V^2, calculate the value of I_1. (2 pts)

(c) If the circuit output operates like a class-AB stage, explain the purpose and operation of transistors N_2, P_2, and resistors R_a, R_b. (3 pts)

(d) If $R_a=R_b=R$=200Ω, and the other parameters are the same as in (2), calculate the maximum current flowing through the transistor P_1. (4 pts)

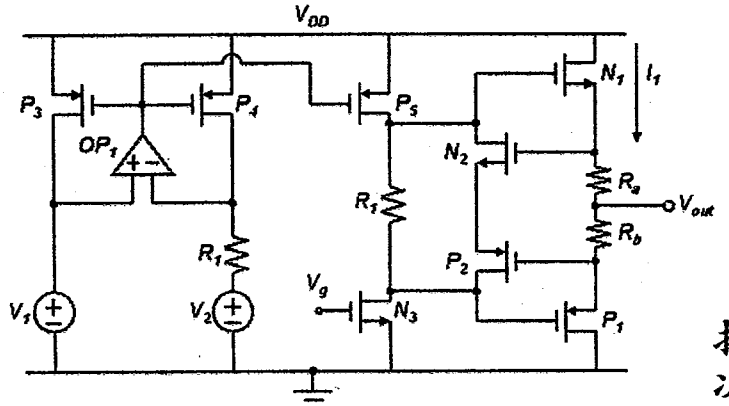

Fig. 4

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5. For the circuit below (see Fig.5), P_1=P_2, P_3=P_4, and N_1=N_2, N_3=N_4. The size of transistor N_3 is N times of N_1. Let k_n'=100μA/V^2, k_p'=40μA/V^2, C_{ox}=5fF/μm^2, $|V_{tp}|$=V_{tn}=1V. Ignore the body effect, but consider the channel-length modulation effect. The transistor Early voltages (V_A) for P_1, P_3, N_1 and N_3 are 10V, 250V, 50V, and 50V, respectively. The common-mode feedback network is not shown for simplicity. Assume the circuit is properly biased. Express the calculated gain in dB for the following questions.

(a) If I_A is 0 and N is 1, calculate the DC gain (A_v=(V_{op}-V_{on})/(V_{ip}-V_{in})) and the gain-bandwidth product (GBW) of this circuit. (3 pts)

(b) If N is changed to 5, while I_A is still 0, what are the DC gain (A_v) and the GBW? (3 pts)

(c) Compare the answers you get in (1) and (2), explain what happens when N is changed from 1 to 5, while I_A is 0? (3 pts)

(d) If I_A is 0.375mA and N is 5, what are the DC gain (A_v) and the GBW? (3 pts)

(e) Where is the location (which node) of the non-dominant pole? Estimate the non-dominant pole frequency for I_A=0.375mA and N=5. (4 pts)

(f) If I_A is increased and is close to 0.5mA, what will happen to the DC gain (A_v) and the phase margin of the circuit (improve or degrade)? You must state your reasons. (4 pts)

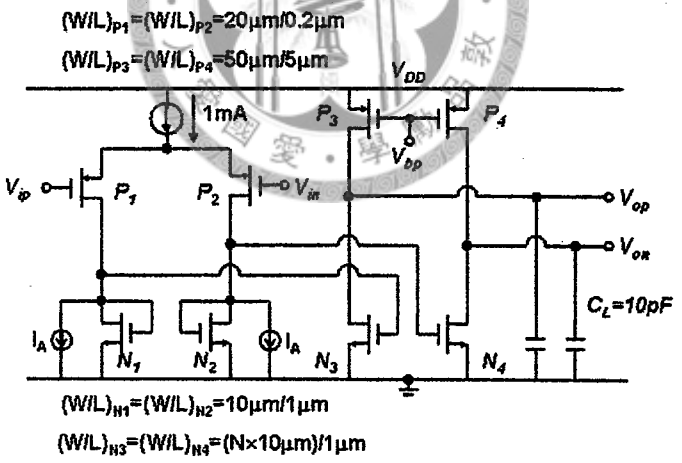

Fig. 5

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