

※ 注意：請於試卷上「選擇題作答區」依序作答。

選擇題 32 題，連連看 18 題。

1. (2pts) Suppose that we have a CPU instruction TestAndLock that supports the implementation of access control to critical sections. The following program template shows how we can use the instruction to implement the mutual exclusion requirement to critical section. L is a static integer variable with initial value zero.

```
while (1) {  
    while (TestAndLock(&L)) ;  
    /* critical section. */  
    L = 0;  
    /* remainder section. */  
}
```

Please tell us which one of the following is a correct implementation of TestAndLock() in micro-instructions? Note each CPU instruction is atomic, that is, the intermediate results between the micro-instructions of the CPU instruction is not available to other CPU instructions.

- (A) int TestAndLock(int \*lock\_ptr) {  
 while (\*lock\_ptr == 1) ;  
 \*lock\_ptr = 1;  
 return 0;  
}
- (B) int TestAndLock(int \*lock\_ptr) {  
 \*lock\_ptr = 0;  
 while (\*lock\_ptr == 1) ;  
 \*lock\_ptr = 1;  
 return 1;  
}
- (C) int TestAndLock(int \*lock\_ptr) {  
 if (\*lock\_ptr == 1)  
 return 1;  
  
 else  
 return 0;  
}
- (D) int TestAndLock(int \*lock\_ptr) {  
 if (\*lock\_ptr == 1)  
 return 1;  
 \*lock\_ptr = 1;  
 return 0;  
}
- (E) int TestAndLock(int \*lock\_ptr) {  
 if (\*lock\_ptr == 1)  
 return 1;  
 while (\*lock\_ptr == 0) ;  
 return 0;  
}

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2. (2pts) With the implementation of the correct answer to question 1 in the above, there are the following three properties of the program template that we want to check.

- (a) The bounded waiting property.
- (b) The progressiveness property.
- (c) No interrupt will be missed in the critical section access control.

Which of the three properties are true ?

- (A) a, b, c
- (B) a, b
- (C) b, c
- (D) a, c
- (E) None.

3. (2pts) Assume we are using the time-stamp based protocol to control the concurrency among five transactions. Assume that we have five transactions, P1, P2, P3, P4, and P5. We also have five variables A, B, C, D, and E. In the following table, we have recorded a schedule.

time	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
P1	TS	RA						RC			WC						WE
P2			TS			RB				RC					RD	RC	
P3				TS	WA												
P4							TS		RC					WA			
P5												TS	RD				

The first row records the time-stamps while the other rows record the operations of transactions at a particular time. An entry 'TS' at the row of P<sub>i</sub> at time k means that at time k, transaction P<sub>i</sub> starts. An entry 'WX' at the row of P<sub>i</sub> at time k means that transaction P<sub>i</sub> writes to variable X at time k. An entry 'RX' at the row of P<sub>i</sub> at time k means that transaction P<sub>i</sub> reads variable X at time k. What is the value W-timestamp(A) at time 14 ?

- (A) 0
- (B) 3
- (C) 4
- (D) 6
- (E) 13.

4. (2pts) According to the schedule in question 3, what is the value of R-timestamp(C) at time 10 ?

- (A) 2
- (B) 6
- (C) 7
- (D) 8
- (E) 9.

5. (2pts) According to the schedule in question 3, which one of the following is true ?

- (A) Transaction P3 is rejected at time 4.
- (B) Transaction P1 is rejected at time 10.
- (C) Transaction P4 is rejected at time 13.
- (D) Transaction P2 is rejected at time 14.
- (E) No rejection is generated in the schedule.

6. (2pts) In the following, we have five properties:
- (a) efficiency in context switching
  - (b) efficiency in information hiding
  - (c) efficiency in thread creation
  - (d) efficiency in message-passing
  - (e) convenience in memory sharing.
- Which ones are not the advantage of user threads over kernel threads ?
- (A) b,d,e
  - (B) a,b,e
  - (C) a,c
  - (D) b,d
  - (E) c,d,e.
7. (2pts) Which statement is true?
- (A) Cache management is a key issue in the processor affinity policy.
  - (B) hyper-threading is a new library that allows us to construct a hierarchy of threads for better class inheritance.
  - (C) Processor affinity is a new metric that allows us to evaluate the physical distance between two processors in the migration of processes.
  - (D) Multi-core systems can alleviate the problem of data race because many threads can now run in parallel.
  - (E) In a dual-core computer, the performance of a multi-thread program can easily be doubled.
8. (2pts) Which statement is true ?
- (A) After a user program starts an I/O operation, it has to wait for the completion of the I/O operation to resume its program execution.
  - (B) Interrupt vector tells us the port addresses of the I/O controllers.
  - (C) DMA needs to work with device polling mechanism.
  - (D) Data movement between I/O devices and the main memory usually are executed in CPU to enhance the I/O performance.
  - (E) Interrupt handling starts with saving the current context.
9. (2pts) Which of the following statement regarding the process of starting computers is correct ?
- (A) Boot block happens when some hardware problem blocks the process of starting a computer.
  - (B) If we have a boot block, then we need to wake up the operating systems to check what problem has happened.
  - (C) A boot block is there because we need to use it to find the bootstrap program.
  - (D) Boot blocks need to be recorded in the RAM when we need them.
  - (E) After the bootstrap program finishes, the operating system is ready to execute the commands from users.
10. (2pts) Which of the following statements is true ?
- (A) Thread pool can be used to control the level of multi-programming.
  - (B) Thread pool saves you time in context switching.
  - (C) Thread pool can enhance the load balance among user threads.

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- (D) Only when a thread finishes and leaves the pool, we can allow new threads to enter the pool.  
 (E) A preemptive CPU scheduler may choose a thread to leave the thread pool before the thread finishes.

11. (2pts) Which of the following statements is true regarding CPU scheduling policies ?

- (A) FCFS does not concern with the properties of processes and are only for OS experiments.  
 (B) SJF gives us the best schedulability in practice.  
 (C) SJF is optimal with respect to response time in theory.  
 (D) Round-robin is good for system response.  
 (E) Multi-level feedback queues assign a different priority to each queue so that processes in the lower-priority queues have to wait for the completion of those in the higher-priority queues.

12. (2pts) We have the following hardware devices.

- (a) timers  
 (b) a mode bit  
 (c) register banks  
 (d) page tables  
 (e) limit registers.

Which of the above-mentioned devices can be used to protect system resources ?

- (A) a, b, c, d, e  
 (B) a, b, d, e  
 (C) a, c, e  
 (D) b, e  
 (E) b.

13. (2pts) Which of the following statements is incorrect ?

- (A) Main memory is usually volatile.  
 (B) Cache memory is used in addition to main memory for better storage stability.  
 (C) Disks are used in the storage hierarchy for better storage stability.  
 (D) Disks are used in the storage hierarchy because they are cheaper per bit.  
 (E) The cache coherence problem adds to the complexity of control hardware in storage hierarchy.

14. (2pts) Assume that we have following four processes.

Process	Arrival time	Burst time
P0	0	7 ms
P1	1	3 ms
P2	3	3 ms
P3	5	5 ms

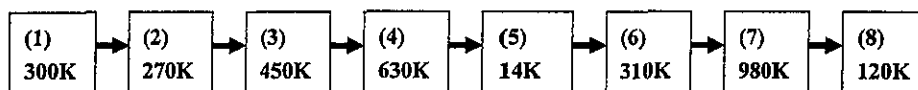
What is the average response time with respect to the FCFS CPU scheduling policy ?

- (A) 48/4  
 (B) 30/4  
 (C) 39/4  
 (D) 29/4  
 (E) 21/4.

15. (2pts) According to question 14, what is the average waiting time when the CPU scheduling policy is Round-Robin with quantum 4 ?

(A) 48/4  
(B) 30/4  
(C) 39/4  
(D) 29/4  
(E) 21/4.

16. (2pts) Assume that we have the following free block list.



We first need a memory space of 540K, then 230K, then 50K, and then 109K. With the Best-Fit policy, we will find the spaces in blocks (a), (b), (c), and (d) in sequence. Note that a, b, c, d are all in [1, 8]. What is the value of  $a^2 + (b+3c)d$  ?

(A) 128  
(B) 68  
(C) 140  
(D) 24  
(E) 30.

17. (2pts) According to question 16, with the Worst-Fit policy, we will find the spaces in blocks (a), (b), (c), and (d) in sequence. Note that a, b, c, d are all in [1, 8]. What is the value of  $a^2 + (3b-c)d$  ?

(A) 32  
(B) 8  
(C) 112  
(D) 20  
(E) 18.

18. (2pts) Assume that we have a virtual memory system (pure page-on-demand) with the LRU algorithm for page replacement. A process has been allocated four physical frames. But this process has ten pages in its logical space. Now we have the following page reference sequence (from left to right) :

(1) (2) (3) (5) (4) (3) (4) (3) (1)

After the page references in the sequence, pages (a), (b), (c), and (d) are in the frames. What is the value of  $a^2 + b^2 + c^2 + d^2$  ?

(A) 30  
(B) 39  
(C) 46  
(D) 51  
(E) 54.

19. (2pts) According to question 18, assume that the OS is using the additional-reference-bits algorithm for LRU approximation. Assume that for each page, we use three bits to record the page reference history. Assume that when there are several pages with all zeros in their reference bits, the OS always chooses the one with the smallest page number to replace. After the page references in the sequence, pages (a), (b), (c), and (d) are in the frames. What is the value of  $a^3 + b^3 + c^3 + d^3$  ?

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- (A) 100
- (B) 161
- (C) 198
- (D) 217
- (E) 224.

20. (2pts) We have a disk with 200 tracks, numbered from 0 to 199. Initially, the disk head is at track 60 and moving in the direction of track 199. Now we have read-write requests to the following tracks:

198, 183, 37, 56

Suppose the OS is using the SSTF disk scheduling policy. Then the disk head will visit the tracks a, b, c, and d in sequence. What is the value of  $3a+4b+c-d$  ?

- (A) 1322
- (B) 1360
- (C) 739
- (D) 331
- (E) 301

21. (2pts) According to question 20, if we are using the C-SCAN disk scheduling policy. What is the travel distance of the disk head ?

- (A) 286
- (B) 258
- (C) 299
- (D) 212
- (E) 301

22. (2pts) We use the Banker's algorithm to do deadlock avoidance. Now the state of resource allocation is described by the following matrices.

	<u>Allocation</u>				<u>Max</u>				<u>Available</u>			
	A	B	C	D	A	B	C	D	A	B	C	D
P0	0	1	0	0	3	2	6	0	4	0	1	1
P1	0	0	0	2	1	2	3	2				
P2	4	0	4	0	4	1	4	3				
P3	0	1	2	0	3	1	2	2				
P4	1	1	0	1	5	1	0	2				

As you can see, there are five processes, P0, P1, P2, P3, and P4. There are also four resource types, A, B, C, and D. From this state information, we can compute the Need matrix as follows.

	<u>Need</u>			
	A	B	C	D
P0	a	b	c	d
P1	e	f	g	h
P2	i	j	k	l
P3	m	n	o	p
P4	q	r	s	t

What is the value of  $a+2f+3k+4p$  ?

- (A) 15
- (B) 16
- (C) 17
- (D) 18
- (E) 19

23. (2pts) According to question 22, assume the safe sequence is  
Pa Pb Pc Pd Pe  
which of the following statements is true ?  
(A) There is not safe sequence in the state.  
(B)  $a+2b+3c+4d+5e=20$   
(C)  $a+2b+3c+4d+5e=21$   
(D)  $a+2b+3c+4d+5e=23$   
(E)  $a+2b+3c+4d+5e=26$ .
24. (2pts) Which of the following statements is true regarding page management ?  
(A) TLB is a key technology in avoiding page faults.  
(B) TLB is crucial in reducing the necessity for checking cache coherence.  
(C) TLB is loaded to the memory when the OS is boot-strapped.  
(D) TLB works to reduce the effective memory access time.  
(E) When TLB cannot find the information the CPU is looking for, the OS will be awoken to load the correct TLB in the disk.
25. (2pts) Which of the following statements is incorrect regarding virtual memory management ?  
(A) Working set model can help control the level of multiprogramming.  
(B) When a process is not allocated enough frames to contain its working set, performance may drop drastically.  
(C) OS checks the program of each process to calculate its working set for the duration of the process execution.  
(D) Locality of memory reference is crucial to the performance of virtual memory management.  
(E) The copy-on-write strategy can save precious time in process creation.
26. (2pts) \_\_\_\_\_ implements the translation of a program's address space to physical addresses.  
(A) DRAM  
(B) Main memory  
(C) Physical memory  
(D) Virtual memory
27. (2pts) To track whether a page of cache has been written since it was read into the memory, a \_\_\_\_\_ is added to the page table.  
(A) valid bit  
(B) tag index  
(C) dirty bit  
(D) reference bit
28. (2pts) (Refer to the CPU architecture of **Figure 1** below) Which of the following statements is correct for a LOAD WORD (LW) instruction ?  
(A) MemtoReg should be set to 0 so that the correct ALU output can be sent to the register file.  
(B) MemtoReg should be set to 1 so that the Data Memory output can be sent to the register file.

(C) We do not care about the setting of MemtoReg. It can be either 0 or 1.

(D) MemWrite should be set to 1.

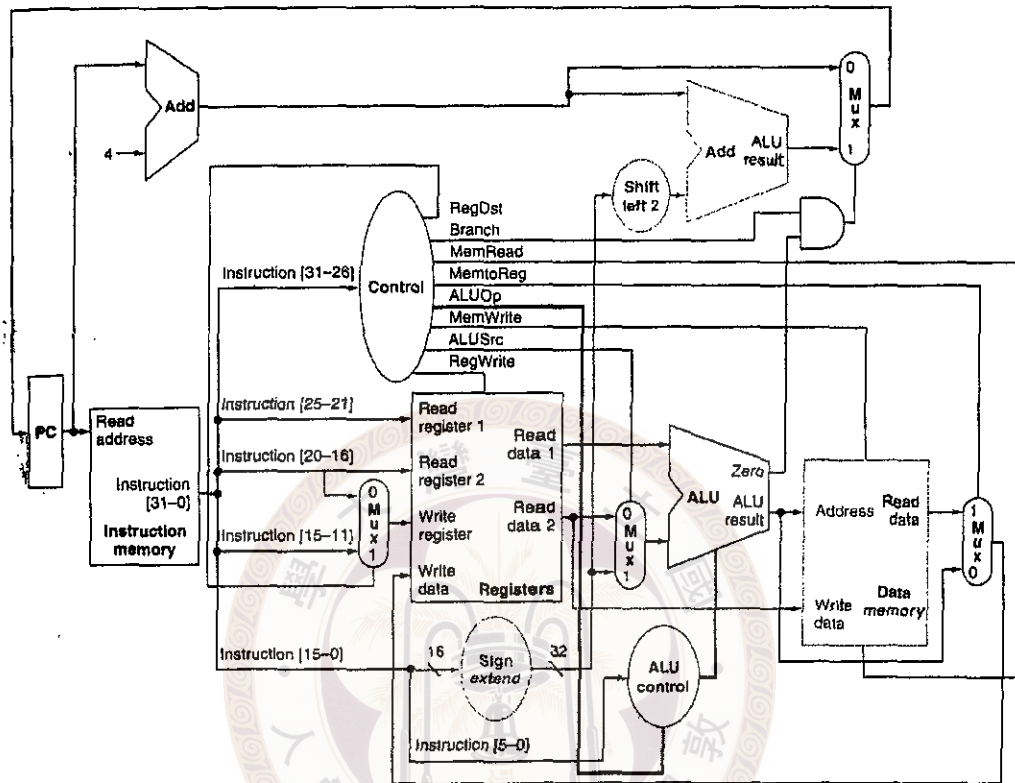


Figure 1

29. (2pts) The IEEE 754 binary representation of a 32-bit floating number is shown below (normalized single-precision representation with bias = 127)

31	30~23	22~0
S	exponent	fraction
1 bit (S)	8 bits (E)	23 bits (F)

What is the correct binary presentation of  $(-0.75)_{\text{ten}}$  (i.e.,  $-0.75$  in decimal 十進位 notation) in IEEE single-precision float format?

- (A) 1011, 1111, 0100, 0000, 0000, 0000, 0000, 0000  
(B) 1011, 1111, 1010, 0000, 0000, 0000, 0000, 0000  
(C) 1011, 1111, 1101, 0000, 0000, 0000, 0000, 0000  
(D) 1011, 1110, 1000, 0000, 0000, 0000, 0000, 0000

30. (2pts) According to Question 29, what is the decimal number represented by the word below?

Bit Position	31	30~23	22~0
Binary value	1	10000011	011000.....00



- (A) -10
- (B) -11
- (D) -22
- (D) -44

31. (2pts) Assume that the following assembly code is run on a machine with 2 GHz clock. The number of cycles for assembly instruction is shown in Table 1.

	add	\$t0, \$zero, \$zero
loop:	beq	\$a1, \$zero, finish
	add	\$t0, \$t0, \$a0
	sub	\$a1, \$a1, 1
	j	loop
finish:	addi	\$t0, \$t0, 100
	add	\$v0, \$t0, \$zero

instruction	Cycles
add, addi, sub	1
lw, beq, j	2

Table 1

Assume \$a0=3, \$a1=20 at initial time, select the correct value of \$v0 at the final cycle:

- (A) 157,
- (B) 160
- (C) 163
- (D) 166

32. (2pts) According to Question 31, please calculate the MIPS (millions instructions per second) of this assembly code:

- (A) 1342
- (B) 1344
- (C) 1346
- (D) 1348

Questions 33-36. Link the following terms ((1)~(4))

- (1) Microsoft Word
- (2) Operating system
- (3) Internet
- (4) CD-ROM

to the most related terminology shown below (A, B, C,..., K). Choose the most related one ONLY (answer format: e.g., (1) → K, for mapping item (1) to terminology K).

<b>A</b>	Applications software	<b>F</b>	Personal computer
<b>B</b>	High-level programming language	<b>G</b>	Semiconductor
<b>C</b>	Input device	<b>H</b>	Super computer
<b>D</b>	Integrated circuit	<b>I</b>	Systems software
<b>E</b>	Output device	<b>K</b>	Computer Networking

Please write down the answers in the answer table together with the choice questions.

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(注意：請將答案寫在選擇題作答區，對應題號 33-36 之「A」欄中，否則不予計分)

33. (2pts) (1) Microsoft Word → ?  
 34. (2pts) (2) Operating System → ?  
 35. (2pts) (3) Internet → ?  
 36. (2pts) (4) CD-ROM → ?

Questions 37-40. Match the memory hierarchy element on the left with the closest phrase on the right: (answer format: e.g., (1) → d, for mapping item (1) (left) to item d (right))

(1). L1 cache	a. A cache for a cache
(2). L2 cache	b. A cache for disks
(3). Main memory	c. A cache for a main memory
(4). TLB	d. A cache for page table entries

Please write down the answers in the answer table together with the choice questions.

(注意：請將答案寫在選擇題作答區，對應題號 37-40 之「A」欄中，否則不予計分)

37. (2pts) (1) L1 cache → ?  
 38. (2pts) (2) L2 cache → ?  
 39. (2pts) (3) Main memory → ?  
 40. (2pts) (4) TLB → ?

Questions 41-50. Based on the function of the seven control signals and the datapath of the MIPS CPU in Figure 1 (the same figure for Question 28), complete the settings of the control lines in Table 2 (use 0, 1, and X (don't care) only) for the two MIPS CPU instructions (beq and add). X (don't care) can help to reduce the implementation complexity, you should put X whenever possible.

Instruction	Branch	ALUSrc	Reg Write	RegDst	MemtoReg	Memory Write	Memory Read	ALUOp1	ALUOp0
beq	(41)	(42)	(43)	(44)	(45)	(46)	(47)	1	0
add			(48)		(49)	(50)			

Table 2

Please write down the answers in the answer table together with the choice questions.

(注意：請將答案寫在選擇題作答區，對應題號 41-50 之「A」欄中，否則不予計分)

41. (2pts) (41) = ?  
 42. (2pts) (42) = ?  
 43. (2pts) (43) = ?  
 44. (2pts) (44) = ?  
 45. (2pts) (45) = ?  
 46. (2pts) (46) = ?  
 47. (2pts) (47) = ?  
 48. (2pts) (48) = ?  
 49. (2pts) (49) = ?  
 50. (2pts) (50) = ?

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