＊下列題目請在試卷內的「非選擇題作答區」作答。

1. (40%) The circuit in Fig. 1-1 is a fully differential op amp with $V_{tn} = |V_{tp}| = 1$ V, $\mu_n C_{ox} = 200\ \mu A/V^2$, $\mu_p C_{ox} = 100\ \mu A/V^2$, $|V_A| = 100$ V, $(W/L)_1 = (W/L)_2 = (W/L)_3 = (W/L)_4 = (W/L)_7 = (W/L)_8 = (W/L)_9 = (W/L)_{10} = 2$, and $(W/L)_5 = (W/L)_6 = (W/L)_{11} = 4$.
   (1) (8%) Find the input common-mode range (ICMR).
   (2) (8%) Find the output swing.
   Note that the op amp can also be presented as the simplified model in Fig. 1-2.
   (3) (8%) Find the transconductance G_m.
   (4) (8%) Find the output resistance R_o.
   (5) (8%) Find the differential-mode voltage gain $A_v \equiv v_o/v_i$.
   [Hint: channel length modulation can be neglected in the dc analysis]

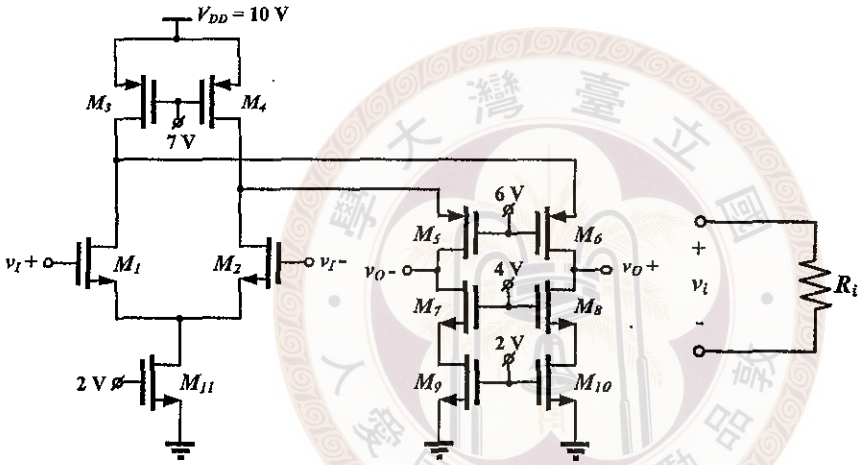

Fig. 1-1

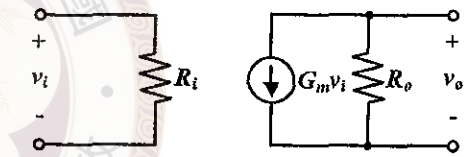

Fig. 1-2

2. (20%) Consider the circuit in Fig. 2 with $v_I = 2 + 0.01 \times cos(100t)$ V and output saturation levels $L_+ = 5$ V and $L_- = -5$ V.
   (1) (10%) Given that $R_1 = 20$ kΩ, $R_2 = 30$ kΩ, $R_3 = 40$ kΩ and $R_4 = 10$ kΩ, find the output voltage v_O (including the dc and the ac components).
   (2) (10%) Given that $R_1 = 20$ kΩ, $R_2 = 30$ kΩ, $R_3 = 10$ kΩ and $R_4 = 40$ kΩ, find the output voltage v_O (including the dc and the ac components).

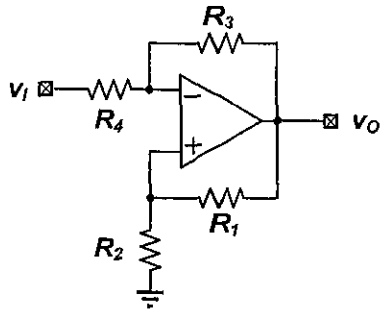

Fig. 2

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3. (20%) Consider the logic-circuits in Fig. 3-1 and 3-2.
   (1) (10%) The circuit in Fig. 3-1 is a dynamic logic gate, which is in the precharge phase when $\varphi = 0$ and in the evaluation phase when $\varphi = V_{DD}$. Please express the logic function Y.
   (2) (5%) The one in Fig. 3-2 is a CMOS logic circuit. Express the logic function $\overline{Y}$.
   (3) (5%) For the circuit in Fig. 3-2, the aspect ratios of the MOSFETs are provided. If we want to have the worst-case t_{PHL} identical to the worst-case t_{PLH}, what is the required ratio of $\mu_n C_{ox}$: $\mu_p C_{ox}$?

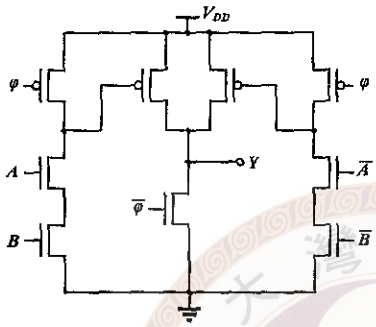

Fig. 3-1

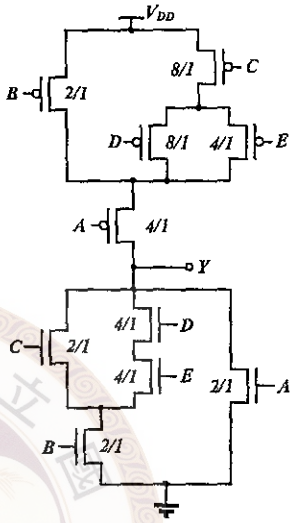

Fig. 3-2

4. (20%) The circuit in Fig. 4 is a 4-bit DRAM where C_{S1}-C_{S4} are used as the memory cells and C_{D1}-C_{D2} are the dummy cells. When $\varphi = V_{DD}$, the circuit is in the precharge phase. By selecting the associated word line with a high voltage of V_{DD}, the READ and WRITE operations can be performed when $\varphi = 0$ V. Note that V_{DD} is 5 V and the threshold voltage of the MOSFETs is 1 V. Assume that capacitors in the cells are identical, and the equivalent capacitance of each one of the bit lines is 100 times as large as the cell capacitors.
   (1) (5%) If one would like to WRITE logic "1" into cell 1, what is the voltage across C_{S1}?
   (2) (5%) If one would like to WRITE logic "1" into cell 3, what is the voltage across C_{S3}?
   (3) (5%) If logic "1" is stored in cell 1, what is the voltage at B for READ operation?
   (4) (5%) If logic "1" is stored in cell 3, what is the voltage at $\overline{B}$ for READ operation?
   [Hint: Neglect the sense amplifier]

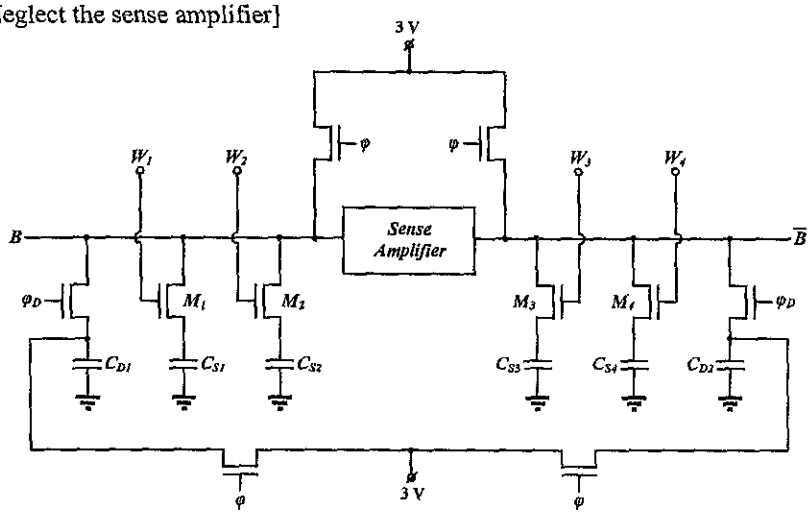

Fig. 4

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