＊下列題目請在試卷內的「選擇題作答區」作答。

一、單選選擇題（20%，每題 2%，不倒扣，答案卷上需按題號答題，否則不予計分）

1. Which of the following mechanism can be observed for the carrier movement within un-biased pn-junction? (A) emission; (B) diffusion; (C) convection; (D) hopping.

2. For a p-n junction under equilibrium condition, which of the following phenomena can NOT be observed? (A) The majority carriers flowing across the junction; (B) The depletion region formed near the junction; (C) The minority conversion layer formed near the junction; (D) The built-in potential formed across the junction.

3. "Early effect" and "channel length modulation" are commonly observed in modern transistor devices. Which of the following properties is NOT caused by such effects? (A) The base width of the BJT is reduced; (B) The turn-on voltage of MOSFET is reduced; (C) The channel of the MOSFET is pinch-off; (D) The emitter current of the BJT is increased.

4. The temperature is extremely important to determine the operational characteristics of the electronics. Which of the following is NOT TRUE if the environmental temperature is raised? (A) It is harder to induce channel in the MOSFET; (B) The saturation current of the BJT is reduced; (C) The characteristics of MOSFETs are shifted more than BJTs; (D) The temperature compensation can be implemented by circuit designs.

5. The operational amplifier is one of the major electronic components in this era. Which of the following description is NOT TRUE for the operational amplifier? (A) In ideal Op Amp, the input impedance is infinite and the output impedance is zero; (B) In ideal Op Amp, the common-mode rejection is infinite and open-loop gain is infinite; (C) In real situation, the open-loop gain is finite and increases with frequency; (D) Op amps are prone to DC problems such as DC offset and input bias.

6. Which one could be the reason for distorted waveforms at the amplifier output? (A) low input impedance; (B) low output impedance; (C) insufficient voltage gain; (D) insufficient bandwidth.

7. Which one of the statements is NOT TRUE? (A) All ac sources should be neglected in DC analysis; (B) Capacitors are considered short circuits in ac analysis; (C) DC voltage sources are considered ac ground; (D) DC current sources are considered open in ac analysis.

8. For crystal oscillators, which one of the following is NOT TRUE? (A) It can operate at higher frequencies than opamp-based oscillators; (B) The oscillation frequency is mainly determined by ω_s of the crystal; (C) The oscillation frequency is determined by ω_p of the crystal; (D) It can provide more stable oscillation output than LC oscillators.

9. For an analog signal with maximum voltage amplitude of 10 V, what is the minimum requirement for the ADC to achieve a resolution of 0.01 V? (A) 4-bit (B) 6-bit (C) 8-bit (D) 10-bit.

10. For a pnp transistor at saturation, which one of the following statements is NOT TRUE? (A) Forward bias at both junctions; (B) The direction of I_E must be out of the emitter; (C) The direction of I_B must be out of the base; (D) The direction of I_C depends on the junction bias.

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＊下列題目請在試卷內的「非選擇題作答區」作答。

二、計算、問答題

1. (20%) Find the transfer characteristics of the closed-loop opamp circuit in Fig. 1(a).
   (1) (5%) Using the opamp as shown in Fig. 1(b).
   (2) (5%) Using the opamp as shown in Fig. 1(c).
   (3) (10%) Using the opamp as shown in Fig. 1(d).
   [Please provide necessary calculations and sketch v_O versus v_I with all the details.]

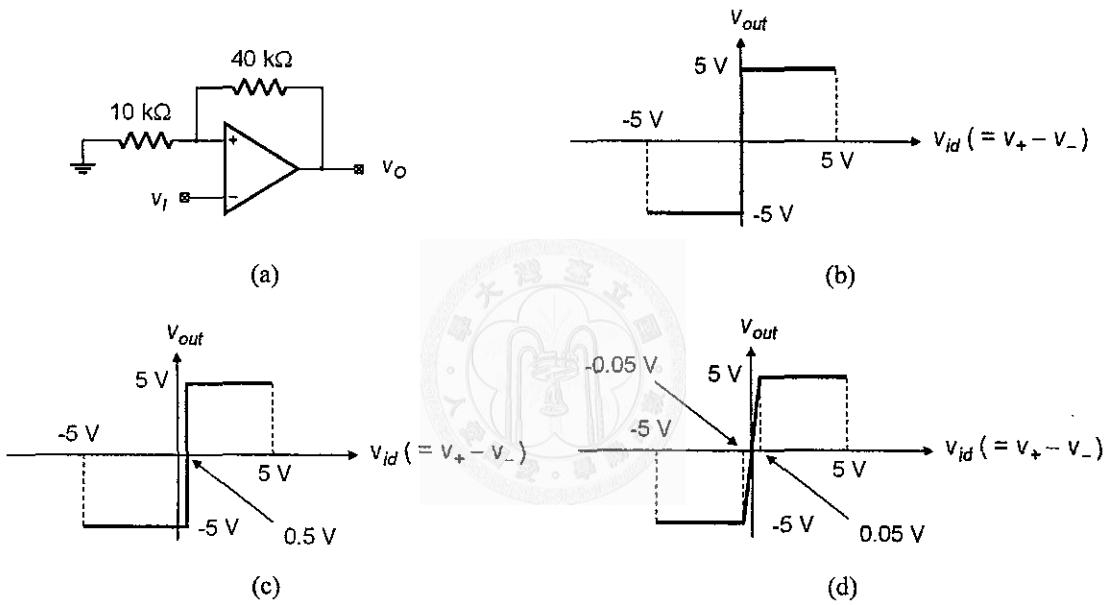

Fig. 1

2. (20%) Please find v_{O1}/v_S and v_{O2}/v_S for the circuit in Fig. 2.
   (1) (5%) Assume the opamps are ideal.
   (2) (15%) Assume the opamps have a finite voltage gain of A_{v0}.

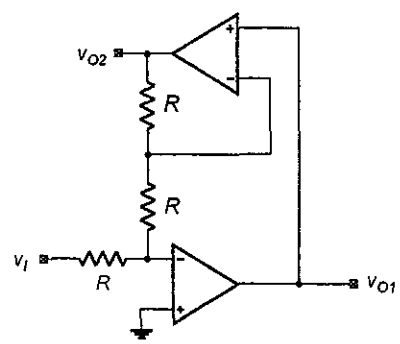

Fig. 2

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3. (20%) As shown in the following figure, it is the active-loaded MOS differential pair. This circuit is one of the most populous input stages for Op Amps. Assume all transistors in this figure are the same. Given the condition shown as follows, please design the required circuit for the following questions. (Please make the necessary assumptions as you write down the equation. It should be noted that the point will be taken off if they are pop-up equations and answers)
Conditions: For all transistors in the following figure (except specially noted in the figure). W/L = 1μm/0.3μm, C_{gs} = 20 fF, C_{gd} = 5 fF, C_{db} = 5 fF, $\mu_n C_{ox}$ = 400 μA/V^2, $\mu_p C_{ox}$ = 90 μA/V^2, $|V_A|$ = 5 V, I = 0.2 mA, R_{ss} = 20 kΩ, the loading capacitance of the following circuit is 25 fF.

   (1) (15%) It is clear that the voltage gain of the differential input stage is not enough to be the Op Amp solely. We have to design the second amplification stage or even the third stage for the better performance. Please design the second stage (consists only active devices, transistors) connected to the circuit to obtain a total dc gain of 100 V/V. Please draw the circuit of your design and calculate the W/L ratio of the transistors in the second stage ($I_{D\,(2nd\ stage)}$ = 0.5 mA; for simplicity, assume the channel length of the second stage is 1 μm).

   (2) (5%) If the dc gain you have designed previously is enough for the specific application, however, this circuit is not stable within the required frequency range. To improve the circuit frequency performance, it is necessary to provide a dominant pole to this 2-stage amplifier you designed previously. Please use the feedback concept and add the minimum number of passive components to achieve it and draw the small-signal equivalent circuit for it and specify the sources of different capacitors in your drawing.

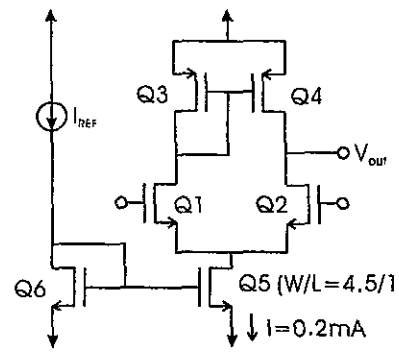

Fig. 3

4. (20%) BJT structure has occupied the important role in circuit designs especially in high speed and power handling circuits. As the consequence, it is necessary to understand the detail analysis of BJT circuit. Start from the basic BJT circuit, such as single stage CE amplifier shown in the following figure. The common emitter current gain is 120 and the thermal voltage is 25 mV.
   (1) (6%) Find the quiescent values of the bias current I_B and I_C.
   (2) (4%) Determine the small-signal input resistance between base and emitter, looking into the base.
   (3) (4%) Obtain the open circuit voltage gain $A_V = V_l/V_S$ as the switch S is opened by using the small

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signal model analysis.

(4) (6%) As the S is closed, loading applied, it is desired to have a lower 3 dB frequency at 10 Hz. Determine the value of C_1 and obtain the voltage gain at mid-band frequency.

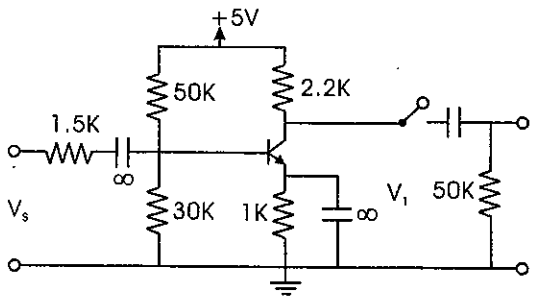

Fig. 4