1. Figure 1(a) is the cross-section of an enhancement-type MOSFET. **(12%)**
   (a) Write the full name of MOSFET in English.
   (b) Is this NMOS transistor PMOS transistor in Fig. 1(a)?
   (c) Apply the voltages in drain, source and gate and ground the body, we get the i_D-v_{SD} characteristics as shown in Fig. 1(b). For the operating points A, B, C, D in Fig. 1(b), plot the depletion region and the channel in Fig. 1(a) for each operating point.

2. Figure 2 shows a discrete-circuit common source amplifier. The input signal v_{sig} is coupled to the gate through a very large capacitor (shown as infinite). The transistor source is connected to ground at signal frequencies via a very large capacitor (shown as infinite). The output voltage signal that develops at the drain is coupled to a load resistance via a very large capacitor (shown as infinite). **(15%)**
   (a) If the transistor has V_t = 1V, and $k_n'W/L$ = 2mA/V^2, verify that the bias circuit establishes V_{GS} = 2V, I_D = 1mA, and V_D = +7.5V. That is, assume these values, and verify that they are consistent with the values of the circuit components and the device parameters.
   (b) Find g_m and r_o if V_A = 100V.
   (c) Draw a complete small-signal equivalent circuit for the amplifier assuming all capacitors behave as short circuits at signal frequencies.
   (d) Find R_{in}, v_{gs}/v_{sig}, v_o/v_{gs}, and v_o/v_{sig}.

3. In Fig. 3, consider the circuit for the case: I = 200 μA and V_{OV} = 0.25 V, R_{sig} = 200 kΩ, R_D = 50 kΩ, C_{gs} = C_{gd} = 1 pF. Find the dc gain, the high-frequency poles, and an estimate of f_H. **(15%)**

4. In Fig. 4, find the voltages at all nodes and the currents through all branches in the circuit. Assume $|V_{BE}|$ = 0.7V and β = ∞. **(15%)**

5. Figure 5 is the CMOS op amp which is fabricated in a process for which V'_{An} = 25 V/μm and $|V'_{Ap}|$ = 20 V/μm. Find A_1, A_2, and A_v if all devices are 0.8-μm long and are operated at equal overdrive voltage of 0.25-V magnitude. Also, determine the op-amp output resistance obtained when the second stage is biased at 0.4 mA. What do you expect the output resistance of a unity-gain voltage amplifier to be, using this op amp? **(15%)**

6. Figure 6 is a *pn* junction diode. **(15%)**
   (a) Plot the carrier concentration p and n, charge density N_D and N_A, electric field, and electric potential as a function of x.
   (b) What is the physical origin or meaning of minority-carrier lifetime?
   (c) If p region is more heavily doped than the n region, i.e., $N_A >> N_D$, plot the minority-carrier distribution and the depletion region in a forward-biased *pn* junction.

7. An amplifier has the voltage transfer function $T(s) = \dfrac{10s}{(1+s/10^2)(1+s/10^5)}$ **(13%)**
   (a) Find the poles and zeros.
   (b) Sketch the Bode magnitude plot for this amplifier.
   (c) Sketch the Bode phase plot for this amplifier.
   (d) Find approximate values for the gain at ω=10, 10^3 and 10^6 rad/s.

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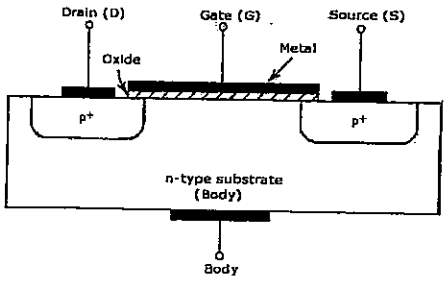

Fig. 1 (a)

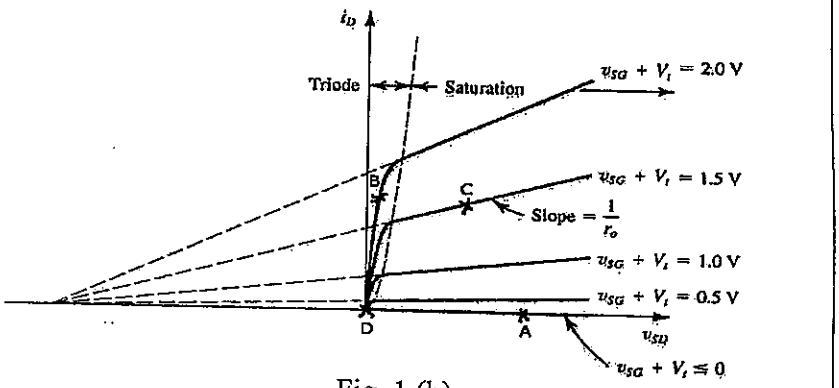

Fig. 1 (b)

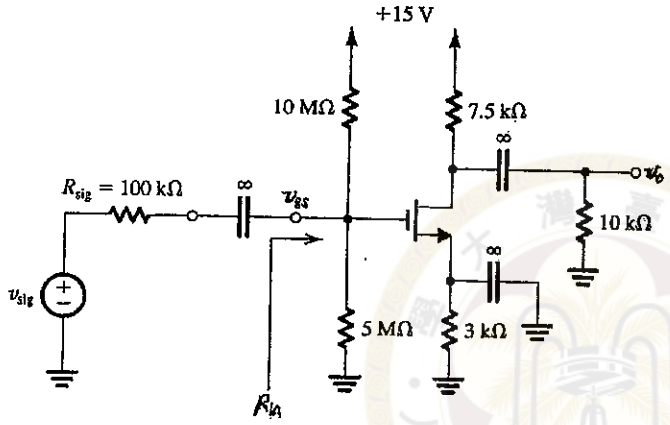

Fig. 2

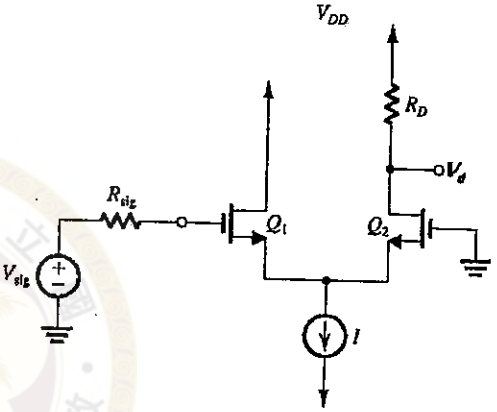

Fig. 3

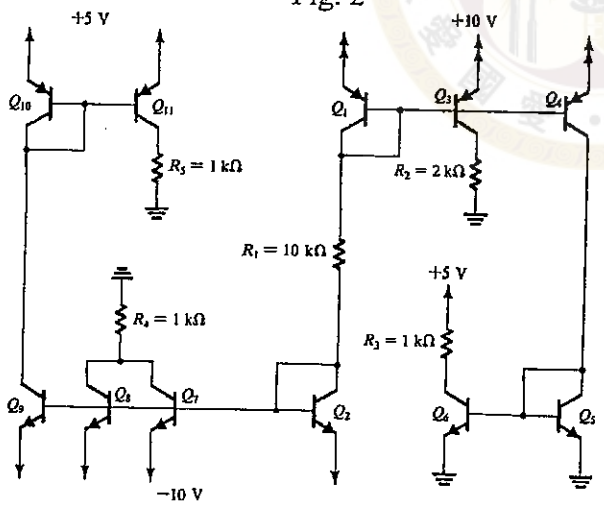

Fig. 4

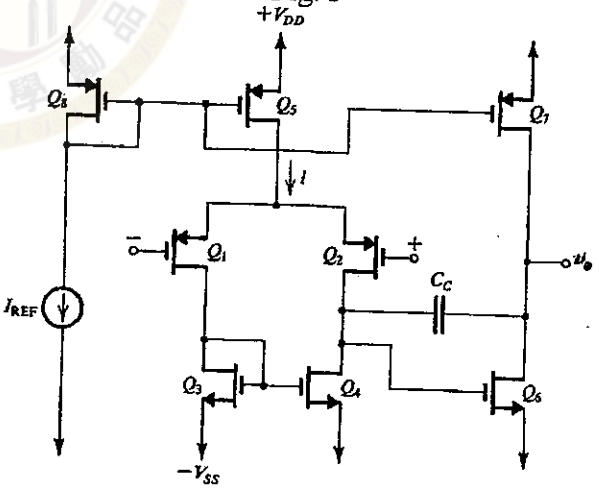

Fig. 5

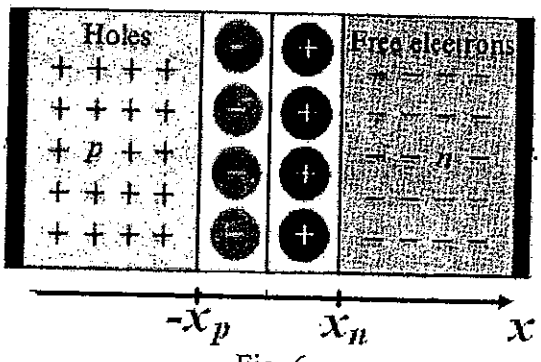

Fig. 6

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