題號:413

## 國立臺灣大學98學年度碩士班招生考試試題

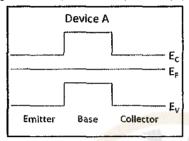
科目:電子學(丁)

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## ※ 注意:請於試卷內之「非選擇題作答區」依序作答,並應註明作答之大題及小題題號。

- 1. The operation of the bipolar junction transistors (BJTs) utilizes the controllable carrier transport through the base region. The band structures of two different BJT devices without any bias voltage are shown in Fig. 1. Both of them have the same base widths and similar device sizes.
  - (a) In the normal operation, what is the type of carriers (electron or hole) which dominate the current flow through the base in the Device A? Please explain why. (5%)
  - (b) Which device (A or B) would possess higher operation speed (mainly dominated by the transport time through the base)? Please explain why. (10%)



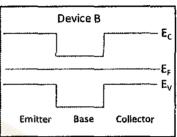
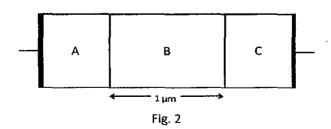


Fig. 1

2. A junction diode is shown in Fig. 2. The doping concentration and type in the regions A, B, and C are 10<sup>18</sup> cm<sup>-3</sup> (n-type), undoped, and 10<sup>19</sup> cm<sup>-3</sup>(p-type), respectively. The temperature is 300K. The intrinsic carrier concentration is 1.5x10<sup>10</sup> cm<sup>-3</sup>, and the dielectric constant is 11.7. The mobility and diffusivity are 500 cm<sup>2</sup>/V-s and 13 cm<sup>2</sup>/s for electron as well as 300 cm<sup>2</sup>/V-s and 8 cm<sup>2</sup>/s for hole, respectively. The minority carrier lifetime is 1 ms in the n-region and 0.5 ms in the p-region.

 $(kT/q = 0.0259V, \epsilon_0 = 8.85 \times 10^{-14} F/cm)$  ln(2)=0.693, ln(3)=1.1, ln(5)=1.6, ln(7)=1.95

- (a) Please calculate the built-in voltage. (5%)
- (b) Please calculate the junction capacitance (per unit area) at zero bias voltage. (10%)
- (c) You calculate the dark current density under various reverse bias voltages by assuming there is no generation or recombination current happening in the depleted region. The results are quite different from the measured data. Which one (calculation or measurement) is higher? Should high or low bias voltage give more difference? What is possible reason to cause the discrepancy? Please explain why. (10%)
- (d) When light is shined on the diode, optical absorption can generate electrons and holes. The electric field in the depleted region can sweep the electrons and holes to be collected as the photocurrent. Please roughly estimate the transport time of the slower carrier, which dominates the device operation speed, when the device is reversely biased at 9 V. (10%)



見背面

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3. For the common-base circuit drawn in Fig. 3, assuming the bias current to be about 1mA,  $\beta$ =100,  $C_{\mu}$ =0.8pF, and  $f_{T}$ =600MHz :

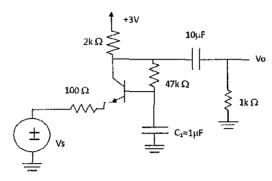


Fig. 3

- (a) Estimate the midband gain Vo/Vs (5%)
- (b) Use the short-circuit time-constants method to estimate the lower 3-dB frequency, f<sub>L</sub>. (5%)
- (c) Find the high-frequency poles, and estimate the upper 3-dB frequency, f<sub>H</sub>. (5%)
- 4. For the operation of the enhancement mode NMOS transistor.
  - (a) What does it mean "enhancement-mode"? (7%)
  - (b) Generally, as we turn on the voltage, the operation of the transistor will be divided to two possible regions. Please describe them and specify the condition of  $v_{ds}$ ,  $v_{gs}$  and  $v_t$  at each region. (8%)
- 5. The circuit in Fig. 4 shows how shunt-series feedback can be employed to design a current amplifier utilizing an op amp.

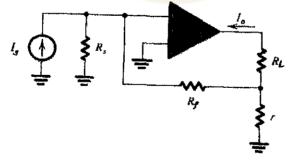


Fig. 4

(a) Show that for large loop gain, the current gain is given approximately by

$$I_o/I_s \sim 1 + (R_f/r)$$
 (5%)

- (b) Using the feedback-analysis method, find
  - the closed-loop gain I<sub>o</sub>/I<sub>s</sub>, (5%) (i)
  - (ii) the input resistance (excluding Rs), (5%)
  - (iii) and the output resistance (excluding RL) (5%)

for the case : open-loop voltage gain of op amp =10<sup>4</sup> V/V,  $R_{id}$  =100k  $\Omega$ , op-amp output resistance =1k $\Omega$ , R<sub>s</sub> = R<sub>L</sub> =10k $\Omega$ , r=100 $\Omega$ , and R<sub>f</sub> =1k $\Omega$ .

## 試題隨卷繳回